Porting commercial-NOS on to Marvell Gen-6 switching ASICs

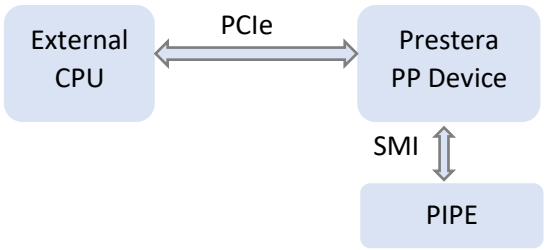
Introduction:

This case study focuses on porting a commercial Network Operating System (NOS) that is already supported on Marvell Gen-5 switching ASICs (AC3X, Aldrin, Aldrin2) to Marvell Gen-6 devices (AC5X/P, Aldrin3, Falcon, etc.). The typical deployment of this NOS is for access and aggregation switches/routers in FTTH networks. The control plane of the NOS supports an exhaustive list of protocols and features required for these deployments.

Marvell-CPSS (SDK) upgrade:

Marvell's CPSS code was upgraded to the latest available to bring in support for Gen-6 devices. The data-plane of the NOS was modified to compile with the new CPSS.

Setup PCIE bus between AC5X and external CPU:

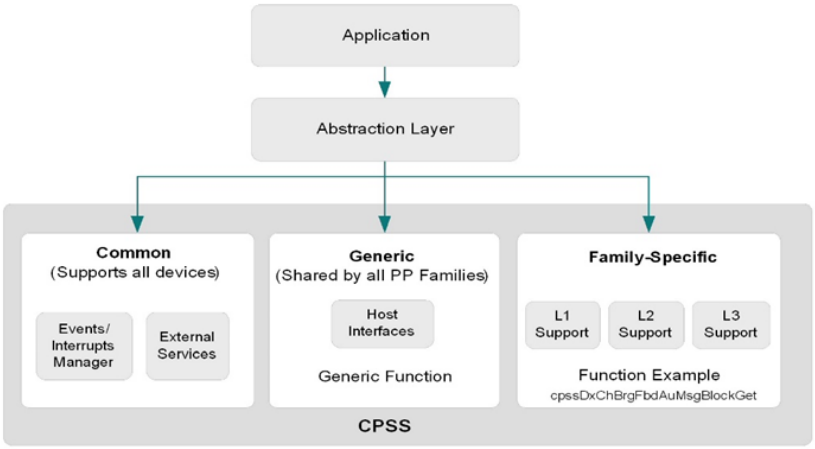


The PCIe bus setup between the AC5X and an external CPU involved the following enhancements to the NOS's PCIe hardware driver:

1. Discover the Prestera-PP device and read the BAR registers.
2. Map CPU memory to the Prestera-PP PCIe BARs.
3. Configure the control and management area with BAR0.
4. Configure the switching core memory with BAR1.
5. Implement PCIe read and write call-back functions for applications.

CPSS Initialization modifications for Gen-6 Devices:

NOS's dataplane application that links with the CPSS code is responsible for initializing various components of the CPSS.



The NOS's data plane application, which links with the CPSS code, is responsible for initializing various components of the CPSS. The initialization process includes:

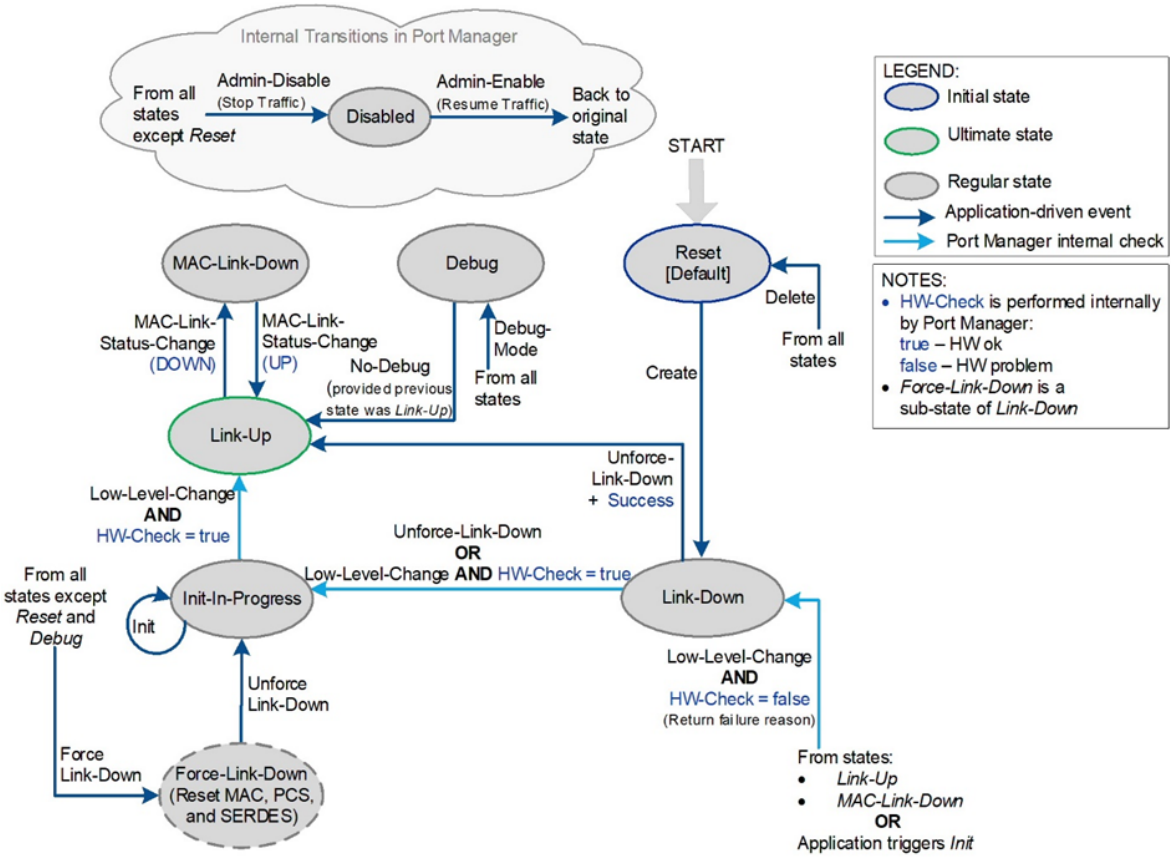
- Pre-Phase 1 Initialization
- Phase 1 Initialization
- Between Phase 1 and Phase 2
- Phase 2 Initialization
- Post-Phase 2 Initialization

This process was modified to accommodate the changes needed for Gen-6 devices. The data plane process of the NOS can now initialize both Gen-5 and Gen-6 devices using the same function, depending on device detection at runtime.

Port-Manager mechanism:

Legacy CPSS APIs for port configuration and management are deprecated for Gen-6 devices. Applications must use the Port Manager APIs for port initialization and link management. The Port Manager is a CPSS port configuration tool for Marvell's switching devices.

A new framework was developed to support the Port Manager, implementing its own state machine. All port configuration and management for Gen-6 devices now use the new APIs provided by the Port Manager, while legacy APIs are still used for Gen-5 devices.



vTCAM Manager support:

Support for the vTCAM Manager was also added as part of this porting. The vTCAM Manager provides a high-level interface between applications and the lower-level CPSS TCAM driver, facilitating easier management and usage of TCAM rules and actions. The interface offers a unified API set that works across multiple devices, TCAM memory sizes, and hardware organizations.

QoS Resource Allocation:

A new mechanism called Dynamic Buffer Allocation (DBA) was introduced for buffer management in Gen-6 devices. DBA dynamically allocates buffers according to ports' and queues' bandwidth requirements and congestion state.

The data plane of the NOS was enhanced to support DBA.

Miscellaneous:

Many CPSS APIs are deprecated or modified for Gen-6 devices. The data plane layer of the NOS was updated accordingly, and all features using these APIs were thoroughly tested for both Gen-5 and Gen-6 devices.